Code No. 2268

FACULTY OF INFORMATICS

B.E. 2/4 (IT) I-Semester (Main) Examination, November / December 2012

Subject : Digital Electronics and Logic Design

Time : 3 Hours **Max. Marks: 75**

Note: Answer all questions of Part - A and answer any five questions from Part-B.

PART – A (25 Marks)

1. State and prove consensus property. (2)
2. Implement XOR gate using NAND gates only. (2)
3. Mention differences between PAL and PLA. (2)
4. Illustrate practical applications of multiplexers. (3)
5. Differentiate between combinational circuits and sequential circuits. (2)
6. Design JK flip-flop using D flip-flop. (3)
7. Write the basic design steps involved in design of synchronous sequential circuits. (3)
8. Distinguish between Moore FSM and Melay FSM. (2)
9. What is hazard? Explain static and dynamic hazards. (3)
10. Write short notes on "Clock Skew". (3)

PART – B (5x10=50 Marks)

11.(a) Realize the switching function after simplification. (5)

$f(x_1, x_2, x_3)=\Sigma m(1, 3, 4, 5)$

(b) Find the compliment of the function $f(x_1, x_2, x_3)= x_1, x_2, x_3$ and show that $f.f_1=1$ & $f + f_1=1$ (5)

12.(a) Explain the architecture of CPLD. (5)

(b) Design 2x4 priority encoder. (5)

13.(a) With a neat diagram explain the positive type Master slave edge triggered D flip flop. (6)

(b) Design a 3-bit up counter. (4)

14. Design a counter circuit using sequential circuit approach and implement using D-flip-flop. (10)

15. Analyse the algorithm for division using ASM chart and data path circuit. (10)

16.(a) Express the complements of following function in sum of product form after simplification (use k-map). (6)

$f(x_1, x_2, x_3, x_4) =\Sigma m(0, 2, 6,11, 13, 14)$

(b) What is the significance of look-up tables in an FPGA? (4)

17. Write short notes on :

(a) Counters (3)

(b) Designing a 4 : 1 Multiplexer using 2:1 Multiplexers (3)

(c) Various architectural specification in VHDL (4)

*****