Code No. : 5296

FACULTY OF INFORMATICS
B.E. 4/4 (IT) I Semester (Main) Examination, December 2011
VLSI DESIGN

Time : 3 Hours] [Max. Marks : 75

***Note** : Answer **all** questions from Part **A**. Answer any five questions from Part **B**.*

PART – A **(25 Marks)**

1. Present a general overview of the design hierarchy. **2**

2. Sketch pFET AOI circuit and pFET OAI circuit using pFET rules for the following : **3**

$X = \overline{(a \cdot b) + (c \cdot d)}$

$Y = \overline{(a + e) \cdot (b + f)}$

3. List rules associated with stick diagram layout. **2**

4. Sketch logic diagram and its layout for a non-inverting buffer. **3**

5. Explain cell concept briefly. **2**

6. Illustrate dependence of Midpoint voltage, V_m on the relative device sizes contained in (β_n / β_p) for a pFET. **3**

7. Explain how increasing the device ratio decreases the output low voltage in a pseudo-nMOS. **2**

8. Write the three states of a Tri-state circuit. Sketch CMOS circuit and state where Tri-state circuits are useful. **3**

9. What is a Procedural Block in Behavioral modeling ? Write three types of Timing controls that are used in a Procedural Block. **2**

10. What is an Initialization vector in CMOS testing ? How does this overcome missing a fault in testing ? **3**

PART – B **(50 Marks)**

11. a) Illustrate Bubble pushing using DeMorgan rules. **4**

b) Discuss TG-based exclusive-OR and exclusive-NOR circuits. **6**

12. a) Sketch a circuit and its Layer Patterning for a CMOS Not gate and trace the logic operation on layout. 4

    b) Illustrate the gate capacitance in an n-channel MOSFET using the term, Oxide capacitance. Present a simple linear model for a MOSFET as a linear resistor and derive an approximate equation for current flow. 6

13. a) Describe Lithography. 5

    b) Define Rise Time and Fall Time, and derive the equations for the same. 6

14. a) Describe a Dynamic logic gate using an example. 5

    b) Define Static Noise Margin. Explain writing 1 operation to a static RAM. 5

15. Describe VLSI. Design flow showing Chip-level physical design issues. 10

16. Discuss signal delay as a function of line length, interconnect delay and crosstalk issues in VLSI design. 10

17. Write short note on : 10

    a) Fabrication of CMOS ICS

    b) VLSI Design issues

    c) Testing of VLSI circuits.