

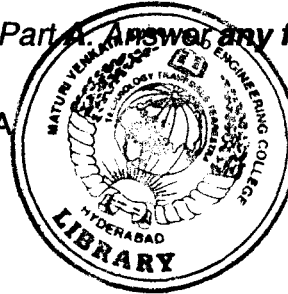
FACULTY OF INFORMATICS
B.E. 2/4 (IT) I Semester (New) (Main) Examination, Dec. 2011
DIGITAL ELECTRONICS AND LOGIC DESIGN

Time: 3 Hours]

[Max. Marks: 75

Note : Answer all questions from Part A. Answer any five questions from Part B.

PART – A



(25 Marks)

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|--|---|
| 1. State and prove Demorgan's laws. | 3 |
| 2. Define Minterm and Maxterm. | 2 |
| 3. Neatly draw the general structure of PLA. | 2 |
| 4. Write the VHDL code for 2×1 multiplexer. | 3 |
| 5. Give the functionality of gated SR latch. | 2 |
| 6. Write the VHDL code for D latch. | 3 |
| 7. What is state-minimization ? | 2 |
| 8. What are the elements of ASM chart ? | 3 |
| 9. Explain dynamic hazard with an example. | 2 |
| 10. Define setup time and hold time of a flip flop. | 3 |

PART – B

(50 Marks)

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|--|----|
| 11.a) Find the Minimum Cost POS form and draw the circuit using NAND gates only.
$f(x_1, x_2, x_3) = \sum m (2, 3, 5, 6, 7, 10, 11, 13, 14).$ | 7 |
| b) Demonstrate by means of truth tables the validity of following identity
$x + yz = (x + y)(x + z).$ | 3 |
| 12. a) With a neat diagram explain general structure of FPGA and its programming. | 7 |
| b) Explain Shannon's expansion theorem. | 3 |
| 13. a) With a neat diagram explain the operation of parallel access shift register. | 6 |
| b) Design a 3-bit down counter. | 4 |
| 14. Explain state-assignment problem with an example. | 10 |
| 15. Analyse the algorithm for shift and add multiplier using ASM chart and datapath circuit. | 10 |
| 16. a) Reduce the expression to minimum-cost SOP form.
$f(x_1, x_2, x_3) = \sum m (0, 1, 3, 7)$ | 4 |
| b) Draw the logic circuit using NAND gates only (after simplification). | 3 |
| c) Write the VHDL code for reduced expression. | 3 |
| 17. Write short notes on : | |
| a) CAD tools | 3 |
| b) Decoders and demultiplexers | 4 |
| c) Flip-flop Vs Latches. | 3 |