Code No. : 3163

FACULTY OF INFORMATICS
B.E. 4/4 (IT) I Semester (Main) Examination, November/December 2010
VLSI DESIGN

Time : 3 Hours] [Max. Marks : 75

*Note : Answer **all** questions from Part –A. Answer **any five** questions from Part–**B**.*

PART – A **(Marks 25)**

1. Realize XOR gate using transmission gate. **2**

2. Explain how a MOSFET works as a switch. **2**

3. Mention different types of MOSFET layers used in layouts. **2**

4. What is latch up problem in CMOS devices ? What is the cause for its occurrence ? **3**

5. Give a RC switch model equivalent for CMOS inverter. **3**

6. Explain 'propagation delay' in an inverter circuit. **3**

7. Define pseudo nMOS. **2**

8. How floor plan effect crosstalk ? **2**

9. Describe Domino Logic. **3**

10. Describe VLSI Design Flow. **3**

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PART – B (50 Marks)

11. a) Derive expression for n-FET current-voltage equations. 5

b) Explain threshold voltage effect in pass characteristics. 5

12. a) Explain Layouts of Basic structure. 5

b) Draw the layout patterns for series and parallel connected FETs. 5

13. a) With neat diagrams explain CMOS process flow. 5

b) Explain DC characteristics of the CMOS inverter. 5

14. a) How the 'Hold' and 'on' operations were performed in Dynamic RAMs ? 5

b) Write about charge leakage in clocked CMOS. 5

15. a) Compare and contrast different high speed adders. 5

b) Write about various test generation methods. 5

16. a) Design an OR-AND PLA that provides the following outputs : 5

$F_1 = M_2.M_3.M_5$

$F_2 = M_0.M_1.M_4$

$F_3 = M_1.M_2.M_6.M_7$

b) Design a 2 to 4 active-law decoder using NOR gates and give the verilog code for the same. 5

17. Explain about **any two** of the following : 5+5

a) Dual rail logic networks

b) Fabrication of CMOS ICs

c) Delay minimization.