Code No. : 3302

FACULTY OF INFORMATICS
B.E. 2/4 (IT) I Semester (Main) Examination, December 2010
DIGITAL ELECTRONICS AND LOGIC DESIGN

Time : 3 Hours] [Max. Marks : 75

Note : *Answer* ***all*** *questions from Part* ***A****. Answer* ***any five*** *question from Part* ***B****.*

PART – A (25 Marks)

1. What is the advantage of a custom chip ? **2**
2. Draw the timing diagram for $f = \overline{x}_1 + x_1x_2$ the input sequence (x_1, x_2) of (0, 0), (0, 1), (1, 0) and (1, 1). **3**
3. Draw the n MOS realization of an AND gate. **2**
4. Differentiate between PAL and PLA. **2**
5. Implement XOR gate using NAND gates only. **2**
6. What is a decoder ? Give the logical diagram of 2-to-4 decoder ? **3**
7. What is meant by edge triggered and level sensitive ? **3**
8. Give the significance of FSN (Finite State Machine). **2**
9. Draw the gated SR latch with NAND gates. **3**
10. List out the fault models. **3**

PART – B (50 Marks)

11. a) Design the simplest product-of-sums circuit that implements the function $f(x_1, x_2, x_3) = \pi M (0, 2, 5)$. **5**

    b) Check the validity of the logic equation

    $$(x_1 + x_3)(\overline{x}_1 + \overline{x}_3) = x_1.\overline{x}_3 + \overline{x}_1.x_3 .$$ **5**

12. a) Compare and contrast between NMOS, CMOS, Bi-CMOS logic circuits. 5

    b) What is a macrocell ? Give the significance of macrocell in CPLD architecture ? 5

13. a) Determine the minimal SOP and POS forms for the function.

    $F(W, x, y, z) = \sum_m (0, 2, 8, 9, 10, 15) + D(1, 3, 67)$. Use K-Maps. 5

    b) Design a four-bit comparator circuit. 5

14. With neat timing diagram explain a four-bit synchronous up-counter. 10

15. a) Explain the Asynchronous behaviour of SR latch. 5

    b) Illustrate path sensitizing with an example. 5

16. Explain design of a counter using sequential circuit approach. 10

17. Write short notes on :

    a) CAD tools. 4

    b) ASM charts. 4

    c) Hazards. 3