Code No. 2332 / N

FACULTY OF ENGINEERING

B.E. 3/4 (EE/Inst.) I – Semester (New) (Main) Examination, Nov. / Dec. 2012

Subject : Digital Electronics and Logic Design

Time : 3 hours **Max. Marks : 75**

Note: Answer all questions from Part-A. Answer any FIVE questions from Part-B.

PART – A (25 Marks)

1. State Demorgam's laws. (2)
2. Using Boolean laws deduce the minimal function of X=(A+B)(A′+C)(B+C). (3)
3. What is an encodes? Give its applications. (2)
4. Find the dual of the function F = X′YZ′ + X′Y′Z. (3)
5. Draw the circuit of a CMOS inverter and briefly explain its operation. (3)
6. Simply the Boolean expression (2)

   F = [(A′+B)(A′+C)(B+C)]′
7. What is the meaning of sourcing and sinking of current? What are its typical values in CMOS logic gates? (3)
8. Add the following numbers using two's complement arithmetic (3)

   a) -90+(-20) b) 125+(-45)
9. Find the maximum length of sequence that can be generated, when four JK flip-flops are used. (2)
10. How is a state diagram useful for designing counters? (2)

PART – B (50 Marks)

11.a) Find the complement of the function

   F = x′yz′ + x′y′z by finding the dual of the function. (4)

   b) Implement NOT, AND, OR, NOR, XOR and XNOR using NAND gates. (6)

12. Explain the following :

   a) TTL family b) RTL family (10)

13.a) Explain about decimal to binary code converter. (5)

   b) Design a 4 to 16 decodes using 3 to 8 decodes. (5)

14. Using J-K flip-flops design a 4-bit asynchronous decade counter. (10)

15. What is the rule of a correcting adder in a BCD adder circuit? Give the circuit diagram of a BCD adder circuit. (10)

16. Design a counter using J-K flip-flop that goes through the states 1, 2, 3, 6, 7 and repeats continuously. (10)

17. Design and draw the PLA implementation of the combinational circuit whose truth table is (10)

Inputs			Outputs	
x	y	z	F_1	F_2
0	0	0	1	1
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	0	0
1	1	0	1	0
1	1	1	1	1

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