Code No. : 5106

FACULTY OF ENGINEERING
B.E. 4/4 (EE/Inst./ECE) (Semester – I) (Main) Examination, December 2011
VLSI DESIGN (Elective – I)

Time : 3 Hours] [Max. Marks : 75

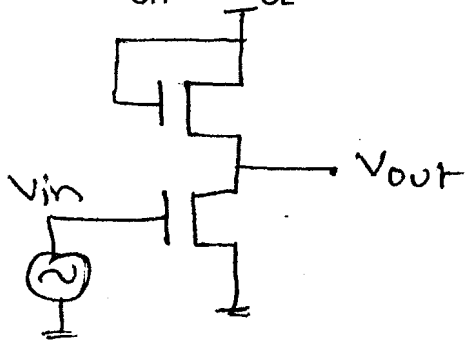
Note : *Answer* ***all*** *questions from Part* ***A****. Answer any* ***five*** *questions from Part* ***B****.*

PART – A **(25 Marks)**

1. Sketch a complementary CMOS gate computing $Y = (A + B) \cdot C$. **3**
2. As the temperature rises, does the current through an 'ON' transistor increase or decrease. Does the current through an 'OFF' transistor increase or decrease ? **2**
3. What are the steps involved in manufacturing IC ? **3**
4. Explain optical lithography. **2**
5. Identify the critical delay path through 2 Half adders. **2**
6. Draw the ckt diagram for a T-type master-slave flip-flop. **3**
7. Under what voltage conditions is a P-transistor with a source connected to $V_{DD} = 5V$ ($V_{tp} = -0.7$ V) a good current source. **2**
8. Compare between CMOS and Bipolar technologies. **3**
9. What is chemical vapour deposition and oxidation ? **3**
10. What are the advantages and applications of current mirror circuit ? **2**

PART – B **(50 Marks)**

11. a) Explain the concept of sheet resistance applied to MOS transistors. **5**
    b) Derive V_{OH} and V_{OL} for the inverter. **5**



12. a) Calculate the approximate dynamic and short circuit power dissipated in a chip operating with a V_{DD} of 5V at 100 MH_3 with an internal switched capacitance of 300 PK (average rise/fall time is 200 ps). 6

    b) How an inversion layer is formed in MOS Transistor ? 4

13. Consider an ALU design

    a) Enumerate all the possible functions of a two-input ALU

    b) For each possible function, list the control inputs to the three function blocks.

    c) Draw the logic circuit. 10

14. a) Explain what is meant by silicon-on-insulator processes, and what are its advantages. 6

    b) Explain about body effect of MOS transistors. 4

15. Explain the process flow for CMOS technology. 10

16. a) Derive the voltage gain and output impedance of common source and common drain amplifier. 6

    b) It is decided to use a mirror ckt to implement a function described in the below truth table

a	b	f
0	0	0
0	1	1
1	0	0
1	1	1

    i) Dose the function have correct symmetry required to build a mirror ckt ?

    ii) If SO construct the logic gate. 4

17. Write short notes on :

    a) Influence of FAN-IN and FAN-OUT on gate design

    b) CAD Tools

    c) Bipolar current mirror. 10