Code No. : 3030

FACULTY OF ENGINEERING

B.E. 3/4 (E&EE/Inst.) I Semester (Main) Examination, December 2010

DIGITAL ELECTRONICS AND LOGIC DESIGN

Time : 3 Hours] [Max. Marks : 75

*Note : Answer **all** questions from Part – A. Answer **five** questions from Part – **B**.*

PART – A **(25 Marks)**

1. Simplify $f(ABC) = A + B' + A'B' + C'B'$. 2

2. Give the karnaugh map for the function
$f(w\,x\,y\,z) = (w' + x + y)\ (w + x' + y')$ 3

3. What are the important features of cmos gates ? Draw a 3-input cmos-NOR gate and its truth table. 3

4. Define an incompletely specified function with an example. 2

5. What is the difference between canonical form and standard form ? 2

6. What type of triggering is incorporated in a master - slave J-K flip - flop ? Explain briefly the triggering phenomenon. 2

7. What is a debouncing switch ? Give the circuit diagram of a debouncing switch. 3

8. Convert J-K flip-flop to 'D' flip-flop. 2

9. Explain the state diagram approach for designing counters. 3

10. Explain fun-in, fun-out and propagation delay. 3

PART – B (50 Marks)

11. a) Obtain the simplified expression of the given expression as a product of sums $F(a, b, c, d) = \pi (0, 1, 2, 3, 4, 10, 11)$

    b) Simplify the given function and implement with NAND gates.

    $fF = AC' + ACE + A'CD' + ACE' + A'D'E'$.

12. Reduce the Boolean expression given below to minimum number of literals using fabulation method and draw the logic circuit diagram.

    $f(w, x, y, z) = \Sigma (0, 1, 2, 8, 10, 11, 14, 15)$

13. a) With the help of a neat circuit diagram explain the operation of a TTL NAND gate. What is an open-collector logic and where is it used ?

    b) Compare the performance of TTL, ECL and CMOS logic gates with reference to fun-in, fun-out, noise immunity and propagation delay. Give typical values in each case.

14. a) Draw the logic diagram of a bounce free manual pulses circuit and explain its operation.

    b) Draw the logic diagram of a 3-bit up/down synchronous counter and explain its operation.

15. Design a 3-bit counter to count the sequence 0, 1, 3, 5, 7, 2, 4, 6 and then repeat using T-flipflops.

16. Briefly explain

    a) Sequence Detectors b) Ring counters

17. a) Insert a full adder circuit with multiplexes.

    b) Design a BCD to excess-3 code converter with a BCD to decimal decoder and four OR gates.