

Code No.: 5142

FACULTY OF ENGINEERING B.E. 3/4 (ECE) I Semester (Main) Examination, Dec. 2011 COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours]	[Max. Marks: 75
Note: Answer all questions of Part A. Answer five questions from Part B.	
PART – A	(25 Marks)
Draw the Block diagram of 4-bit combinational circuit shifter and write in function table.	ts 3
2. Show the hardware for implementing Booth's algorithm.	3
 3. How many clock pubes are required to execute the following micro-ope a) IR ← M[Pc] b) AC ← AC + TR c) DR ← DR + AC 	erations? 3
4. Differentiate between a memory-mapped I/O and an isolated mapped I/	/O 2
5. Explain Flynn's classification of processor.	2
6. Explain Hand-shaking method of Asynchronous data transfer.	3
7. Mention different phases in an instruction cycle.	2
8. What is bootstrap loader?	2
9. Differentiate between complier Assembler and language translator.	3
10. Write briefly about multiprocessor.	2
PART – B	(50 Marks)
 a) Derive an algorithm in flow chart form for the non-restoring method binary division. 	of fixed point 6
 b) Draw the logic diagram of a 4-bit adder-subtracter and explain with of a truth table. 	the help
12. Draw the flow chart for interrupt cycle and explain in detail all the phas	es. 10
13. a) Discuss SIMD processor organization.	4
b) Explain instruction pipeline conflicts and their remedies.	6