FACULTY OF ENGINEERING

B.E. 2/4 (ECE) II Semester (Main) Examination, May/June 2011 **PULSE, DIGITAL & SWITCHING CIRCUITS**

Time : 3 Hours.]

(4)

[Max. Marks: 75

(Marks : 25)

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Note: Answer all questions of Part – A. Answer five questions from Part – B.

PART - A

Sketch the step response of a high pass RC circuit. 1.

(a)

(b)

2. Match the following :

A

- Integrator (1)(2)
 - Attenuator
- Clamper (3) (c)
- Required Diodes and Resistors only Clipper (d)
 - Low Pass RC circuit.

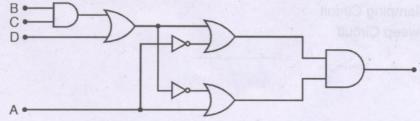
Reduce the amplitude of the signal

Required Diodes, Resistors & Capacitor

- High Pass RC circuit. (e)
- 3. Compare UJT and SCR.
- Draw the circuit of a Schmitt trigger. 4.
- 5. Show the Truth Table for the following function and find its simplest product of sum form :

 $f(x, y, z) = \overline{x} + y\overline{z}$

- Simplify the following algebraic expression : 6. $\overline{WX} + \overline{XY} + \overline{WZ} + YZ$
- 7. Express T as a function of A, B, C, D.



8. Design Half adder with NAND gates only. 3 Convert a JK to D flip-flop. 9. 2 10. Write the excitation table of SR and JK flip-flop. 2 (This paper contains 2 pages) 1 P.T.O.

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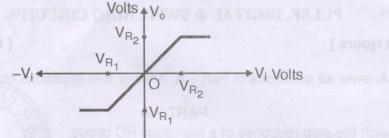
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PART – B

11. (a) Compare Differentiator and Integrator.

(b) Design a circuit to obtain the following transfer characteristic :



- 12. (a) Draw the circuit of a monostable multivibrator and derive an expression for pulse width. 6
 - (b) Plot the waveform at the base and collector of each transistor.
- 13. Find the minimal SOP and POS Expression for the following expression using K-map: 10
 f(w, x, y, z) = ∑m (0, 1, 4, 5, 6, 7, 9, 11, 15) + ∑d (10, 14)
- 14. Design a circuit which converts a BCD code to 7 segment display code. 10
- Design a contact network, with four input relays, w, x, y and z, which receives BCD numbers and produces a signal whenever the present number is 3 or multiple of 3.
- 16. Design a 3 bit synchronous up counter using JK flip-flop. 10
- 17. Write short notes on any two :
 - (a) Symmetric Network
 - (b) Clamping Circuit
 - (c) Sweep Circuit

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