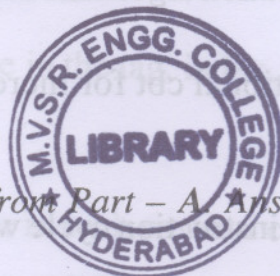




**FACULTY OF ENGINEERING**  
**B.E. 3/4 (ECE) I Semester (Main) Examination, December 2010**  
**COMPUTER ORGANIZATION AND ARCHITECTURE**

Time : 3 Hours]

[Max. Marks : 75



*Note : Answer all questions from Part – A. Answer any five questions from Part – B.*

**PART – A****(25 Marks)**

1. What is the IEEE standard for Binary floating point numbers ? 2
2. The following transfer statement specify a memory. Explain the memory operation in each case.  
a)  $R_2 \leftarrow M[AR]$       b)  $M[AR] \leftarrow R_3$       c)  $R_5 \leftarrow M[R_5]$  3
3. Differentiate between hardwired and microprogrammed control. 3
4. Write the Basic computer instruction formats the memory, register and I/O reference instructions. 3
5. Write the differences between 2 and 3 address instructions. 2
6. Mention the different types of instruction formats. 3
7. Why does DMA have priority over the CPU when both request a memory transfer ? 3
8. List few advantages of the memory - mapped I/O techniques. 2
9. How many 128×8 RAM chips are needed to provide a memory capacity of 2048×16 words ? 2
10. What is mapping and what are the types ? 2



## PART – B

(50 Marks)

11. a) Explain Booths multiplication algorithm with the help of an example. 6
- b) Design a 4 bit combinational cbt for incrementers/decrementers cbt using adders. 4
12. a) Explain the phases of an instruction cycle with necessary control functions and micro - operations. 7
- b) Explain about Von-Neumann machine. 3
13. a) What is an Addressing mode and list the different types ? 5
- b) An instruction is stored at location 300 with its adder field at 301. The adder field has the value 400. A process register R1 contains the number 200. Evaluate the effective address if addressing mode of the instruction is
- i) Direct
  - ii) Immediate
  - iii) Relative
  - iv) Register Indirect
  - v) Index with R1 as the Index Reg. 5
14. a) Explain segmented page mapping technique with the help of a numerical example. 5
- b) Explain associative memory with a neat block diagram and derive the match logic for one word of association memory. 5



15. A digital computer has a memory unit of  $64 \times 16$  and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.
- a) How many bits are there in the tag, index, block and word fields of the address format ? 4
  - b) How many bits are there in each word of cache and how are they divided into functions ? Include a valid bit. 4
  - c) How many blocks can the cache accommodate ? 2
16. a) Design a 4 - bit arithmetic cbt which implements addition subtraction, increment and decrement operations. 5
- b) Draw the block diagram of a micro program sequences and explain. 5
17. Write short notes on :
- a) Interrupts 3
  - b) Asynchronous communication interface. 4
  - c) Virtual memory. 3