

FACULTY OF ENGINEERING

B.E. 2/4 (CSE) I – Semester (Main) Examination, November / December 2012

Subject: Logic and Switching Theory

Time: 3 Hours

Max.Marks : 75

Note: Answer all questions from Part – A. Answer any five questions from Part – B.**PART – A (25 Marks)**

1. Convert the decimal number $(47.625)_{10}$ into binary, octal and hexadecimal. (2)
2. Convert the $(1101011)_2$ to hexadecimal number system. (2)
3. Realize the 4x1 multiplexer using 2x1 multiplexer. (2)
4. Express the function in canonical sum of products form $F(x,y,z) = xy' + yz'$ (2)
5. Convert the given function in sum of max terms $F(x,y,z) = xyz + xy'z'$ (2)
6. Realize full subtractor using Half-subtractor. (3)
7. Draw the minimal contact network for the function $F(x,y,z) = xyz + xyz' + xy'z$ (3)
8. Distinguish between synchronous and asynchronous counters. (3)
9. Realize X-NOR gate using NAND gates. (3)
10. Write the exertation and characteristic table of JK flip flop. (3)

PART – B (50 Marks)

- 11.(a) Simplify the Boolean function using theorems. (5)
 - (i) $ABC + AB' + ABCD + AB'D$
 - (ii) $(x+y)(x+y+z')(x+z+y')$
- (b) Express the complement of the function given in product of Maxterms and draw the $F(x,y,z) = f(0,2,4)$ logic diagram using NAND gates only. (5)
- 12.(a) Simplify the function using K-map method and realize using basic gates only. (5)

$$F(A,B,C,D) = \sum (0,1,2,4,5,8,10,11,14).$$
- (b) Express the function and realize with minimum num of gates (5)

$$F(w,x,y,z) = \sum (1,3,5,7) + \sum_d (4,8,10).$$
13. Design a BCD – to – Excess-3 code converter and realize with minimum no. of gates. (10)
- 14.(a) Design a 4x16 decoder using 2x4 decoders only. (5)
- (b) Write a VHDL-code to design mod-10 counter using JK flip-flops. (5)
- 15.(a) Write a procedure to identify whether a given function is symmetric or not. (5)
- (b) Draw the contact network for the function $F(w,x,y,z) = \sum (1,2,4,6,9,10,11).$ (5)
16. Design a combinational circuit to realize full-adder using NAND-gates only. (10)
17. Write short notes on: (10)
 - (a) Logic synthesis
 - (b) Shift registers.