Code No. : 5342/N

FACULTY OF ENGINEERING
B.E. 2/4 (CSE) I Sem. (New) (Main) Examination, January 2012
LOGIC AND SWITCHING THEORY

Time: 3 Hours] [Max. Marks: 75

Note : *Answer **all** questions from Part **A**, answer **any five** questions from Part **B**.*

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PART – A **(25 Marks)**

1. Convert the decimal number 52.625 into binary, hexadecimal and octal system. **3**
2. Convert the given binary number 11011.101 into BCD number system. **2**
3. Realize a 4 × 16 decoder with two 3 × 8 decoders. **3**
4. Express the function in sum of products and product of sum. **3**

   $F(x, y, z) = x' + x(x + y')(y + z')$.
5. Derive the Even-parity-generator truth table. **2**
6. Realize Half-subtraction. **3**
7. Draw the contact network for the function $F(x, y, z) = \Sigma (1, 3, 5, 7)$. **3**
8. Distinguish between synchronous and asynchronous counter. **2**
9. Differentiate between latch and flip-flop. **2**
10. Realize X-OR gate using NAND gates. **2**

PART – B **(50 Marks)**

11. a) Simplify the Boolean functions to a minimum number of literals : **5**

      i) $xy + x'z + yz$

      ii) $ABC + A'B + ABC'$.

    b) Express the complement of the function given in sum of minterms and draw the logic diagram. **5**

      $F(x, y, z) = \Sigma (0, 3, 6, 7)$.

12. a) Simplify the Boolean function using k-map method and draw logic diagram.

$F(A, B, C, D) = A'B'C' + B'CD' + A'BCD' + AB'C'$.

b) Show that the dual of ex-OR is equal to its complement. **(6+4)**

13. Simplify the function using tabulation method

$F(A, B, C, D) = \sum (1, 2, 3, 5, 7, 9, 10, 11, 13, 15)$ **10**

and realize the function with basic gates.

14. a) Realize full-adder and draw the circuit using NAND gates only.

b) Draw the logic diagram of 4 to 1 line multiplexer with common selection inputs and common enable input. **(7+3)**

15. Design a BCD-to-decimal converter. **10**

16. Design a mod-12 synchronous counter using JK ff. **10**

17. Write short notes on : **(5+5)**

a) Symmetric functions

b) Static hazards.