Code No. : 5343/N

FACULTY OF ENGINEERING
B.E. 2/4 (CSE) I Semester (New) (Main) Examination, December 2011
COMPUTER ARCHITECTURE

Time: 3 Hours] [Max. Marks: 75

Note : *Answer **all** questions from Part A.*
*Answer **any five** questions from Part B.*

PART – A **(Marks : 25)**

1. Perform arithmetic operation with binary numbers with negative numbers in signed 2's complementary form (– 35) + (– 40). **3**

2. Which data structure can be best support using indirect addressing and indexed addressing modes ? **2**

3. Differentiate between CISC and RISC. **2**

4. What is meant by mapping process ? **2**

5. Multiply the following pair of signed 2's complement numbers using bit-pair regarding of the multipliers : A = 010111, B = 101100. **3**

6. Give the instruction format of Vector instruction. **2**

7. How does the processor handle an interrupt request ? **3**

8. What factors influences the bus design decisions ? **3**

9. How do you construct a 8MX32 memory using 512KX8 memory chips ? **3**

10. An eight way set-associative cache consists of a total of 256 blocks. The main memory, contains 8192 blocks. Each consisting of 128 words. Compute the total memory required for cache. **3**

PART – B **(Marks : 50)**

11. Explain in detail about the various instruction formats. **10**

12. What is meant by interrupts ? Discuss in detail about the types of interrupts. **10**

13. Illustrate memory read and write operations. **10**

14. Write the algorithm for division of floating point numbers and illustrate with an example. **10**

15. Draw the typical block diagram of a DMA controller and explain how it is used for direct transfer between memory and peripherals. **10**

16. Describe in detail about the working principles of virtual memory. **10**

17. A computer system has a main memory consisting of 16M words. It also has a 32K-word cache organized in the block-set-associative manner, with 4 blocks per set and 128 words per block.

    i) Calculate the number of bits in each of the TAG, SET and WORD fields of the main memory address format. **6**

    ii) How will the main memory address look like for a fully associative mapped cache ? **4**