Code No. 2076

FACULTY OF ENGINEERING

B.E. 2/4 (CSE) II-Semester **(Main)** Examination, April / May 2013

Subject : **Microprocessors and Interfacing**

Time : 3 Hours Max. Marks: 75

Note: Answer all questions of Part - A and answer any five questions from Part-B.

PART – A (25 Marks)

1. Draw the Flag register of 8085 and write the function of each flag with examples. (2)
2. What is the difference between microprocessor and micro controller? (2)
3. Write control word Register initialization instructions for the 8255 A PPI to set (i) port A as an output port in mode 0, (ii) port B as an output port in mode 1 for I/O (iii) PCU as on O/P in mode 0. (3)
4. What is key bounce? Explain different key bouncing techniques. (3)
5. Mention three differences between 80386 and 80486 micro processors. (2)
6. List out mode in keyboard and display controller 8279 interface. (3)
7. Give the functions of RS 232C Bus. (2)
8. List the 8051 addressing modes. (3)
9. Discuss the criteria for selecting a micro controller device. (2)
10. What is Branch prediction in Pentium processors? (3)

PART – B (5x10=50 Marks)

11. Draw the schematic pin diagram of 8085 MP and explain the various function of the 8085 MPU. (10)

12. (a) Write an ALP program for sorting list of numbers in descending order using subroutines. (5)
    (b) What is a stack and explain the use of stack in sub routines? (5)

13. (a) What is DMA? Explain 8257 DMA controller with a Block diagram. (5)
    (b) List and explain the modes of 8254 interval timer. (5)

14. (a) Draw the Block diagram of 8255 PPI and explain its various modes of operation. (5)
    (b) Explain 8085 vectored interrupts. (5)

15. Explain 8051 micro controller architecture and pin configuration along with memory organization. (10)

16. (a) List the addressing modes of 8086 MP and explain them with examples. (5)
    (b) Explain the memory management of 80386. (5)

17. Write short notes on the following:
    (a) USB (2)
    (b) Real mode and protected mode in Pentium processor (3)
    (c) Modes of 8251 PCI (2)
    (d) Instruction and machine cycle T-states (3)

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