MVSR ENGINEERING COLLEGE – NADERGUL
Department of Electrical & Electronics Engineering
Time Table for B.E. IV Semester (CBCS) EEE (SEC-A) 2017-2018

Room No: M-105 w.e.f. 02/03/2018

DAY	9.30-10.30	10.30-11.30	11.30-12.30	12.30-1.15	1.15-2.15	2.15-3.15	3.15-4.15
Monday	PS-I	EC-II	EM-I	LUNCH	PE	CAED LAB (A) (DHK/GS) / DEIC LAB (B) (KNT/YLN/EVCS)	
Tuesday	MEA	PE	EC-II		EM-IV	EM-I	LIC
Wednesday	CAED LAB (B) (DHK/GS) / DEIC LAB (A) (KNT/YLN/EVCS)		PE		MEA	EM-IV	PS-I
Thursday	EM-IV	EC-II	LIC		PE	EM-I	MEA
Friday	EM-IV	PS-I	EM-I		EC-II	LIC	-----

A,B,C in brackets indicate batches

Legend:

S. No.	Subject Code	Subject		Staff Name
1	BS401MT	EM-IV	Engineering Mathematics - IV	Mr. U. Shanmukha Rao
2	PC401EE	EC-II	Electrical Circuits - II	Mr. C.V.G.K. Rao
3	PC402EE	EM-I	Electrical Machines-I	Dr. E V C Sekhara Rao
4	PC403EE	PS-I	Power Systems-I	Ms. G. Sirisha
5	PC404EE	PE	Power Electronics	Dr. T. Chandra Shekar
6	PC405EE	LIC	Linear Integrated Circuits	Mr. Y.L.N. Rao
7	HS401BM	MEA	Managerial Economics & Accountancy	Mr. Ch. Venkata Rao
8	PC451EE	DEIC LAB	Digital Electronics and Integrated Circuits Lab	Ms. K. Navya Tejaswini / Mr. Y.L.N. Rao / Dr. E V C Sekhara Rao
9	PC452EE	CAED LAB	Computer Aided Electrical Drawing Lab	Dr. D. Harikrishna / Ms. G. Sirisha

Timetable coordinator **Chief Timetable Coordinator** **HOD (EEE)** **Principal**

MVSR ENGINEERING COLLEGE – NADERGUL
Department of Electrical & Electronics Engineering
Time Table for B.E. IV Semester (CBCS) EEE (SEC-B) 2017-2018

Room No: M-106 w.e.f. 02/03/2018

	9.30-10.30	10.30-11.30	11.30-12.30	12.30-1.15	1.15-2.15	2.15-3.15	3.15-4.15
Monday	CAED LAB (A) (BRK/DHK) / DEIC LAB (B) (YLN/VVS/MDV)		PE	LUNCH	EM-I	EC-II	PS-I
Tuesday	CAED LAB (B) (BRK/DHK) / DEIC LAB (A) (YLN/VVS/MDV)		EM-IV		LIC	PS-I	MEA
Wednesday	EM-I	EC-II	LIC		PE	MEA	EM-IV
Thursday	EC-II	EM-I	PS-I		EM-IV	LIC	PE
Friday	PE	EM-IV	MEA		EM-I	EC-II	-----

A,B,C in brackets indicate batches

Legend:

S. No.	Subject Code	Subject		Staff Name
1	BS401MT	EM-IV	Engineering Mathematics - IV	Mrs. D. Bhagya
2	PC401EE	EC-II	Electrical Circuits - II	Mr. V.V. Satyanarayana Akula
3	PC402EE	EM-I	Electrical Machines-I	Dr. D.V.M. Chary
4	PC403EE	PS-I	Power Systems-I	Mr. I. Narasimha Swamy
5	PC404EE	PE	Power Electronics	Dr. T. Chandra Shekar
6	PC405EE	LIC	Linear Integrated Circuits	Mr. Y.L.N. Rao
7	HS401BM	MEA	Managerial Economics & Accountancy	Mr. M. Sriranga Raju
8	PC451EE	DEIC LAB	Digital Electronics and Integrated Circuits Lab	Mr. Y.L.N. Rao / Mr. V.V. Satyanarayana Akula / Ms. M Divya Vani
9	PC452EE	CAED LAB	Computer Aided Electrical Drawing Lab.	Mr. B. Ramakrishna / Dr. D. Harikrishna

Timetable coordinator **Chief Timetable Coordinator** **HOD (EEE)** **Principal**

MVSR ENGINEERING COLLEGE – NADERGUL
Department of Electrical & Electronics Engineering
Time Table for III/IV B.E. II Semester EEE (Sec-A) 2017-2018

Room No: M-205 w.e.f. 02/03/2018

	9.45-10.35	**10.35-11.25**	**11.25-12.15**	**12.15-1.00**	**1.00-1.45**	**1.45-2.35**	**2.35-3.25**	**3.25-4.15**
Monday	MPMC	EM-III	MEA	MEA	LUNCH	SGP	DSP	-----
Tuesday	DSP	MPMC	SGP	MEA		EM LAB-II(A) (NSRK/BRK/MDV) /PE LAB(B) (TCS/GS) /IC LAB(C) (VRK/MRR)		
Wednesday	MEA	SGP	MPMC	DSP		-----	-----	-----
Thursday	EM LAB-II(B) (NSRK/BRK/PBGP/MDV) /PE LAB(C) (TCS/GS/EVCS) /IC LAB(A) (VRK/NR/DSP)			SGP		EM-III	EM-III	-----
Friday	EM-III	EM-III	DSP	MPMC		EM LAB-II(C) (NSRK/BRK/PBGP) /PE LAB(A) (TCS/GS/EVCS) /IC LAB(B) (VRK/NR/DSP)		

A,B,C in brackets indicate batches

Legend:

S. No.	**Subject Code**	**Subject**		**Staff Name**
1	EE 351	DSP	Digital Signal Processing	Mr. G. Satyanarayana / Dr. G. Ravindranath
2	EE 352	EM-III	Electrical Machinery-III	Mr. N.S.R. Krishna
3	EE 353	SGP	Switchgear and Protection	Mr. S. Shyam Mohan
4	EE 354	MPMC	Microprocessors and Microcontrollers	Mr. P.V.V. Raghava Sharma
5	CM 371	MEA	Managerial Economics and Accountancy	Mr. Ch. Venkata Rao
6	EE 381	EM LAB – II	Electrical Machines Lab – II	Mr. N.S.R. Krishna/ Mr. B. Ramakrishna/ Mr. P.B. Guru Prasanna/ Ms. M Divya Vani
7	EE 382	PE LAB	Power Electronics Lab	Dr. T. Chandra Shekar/ Ms. G. Sirisha/ Dr. E V C Sekhara Rao
8	EE 383	IC LAB	Integrated Circuits Lab	Mr. V. Raghukrishna /Mr. N. Ravi/ Mrs. D. Sai Prasanna/Mr. M. Raveendra Reddy

Timetable coordinator **Chief Timetable Coordinator** **HOD (EEE)** **Principal**

MVSR ENGINEERING COLLEGE – NADERGUL
Department of Electrical & Electronics Engineering
Time Table for III/IV B.E. II Semester EEE (Sec-B) 2017-2018

Room No: M-210 w.e.f. 02/03/2018

	9.45-10.35	10.35-11.25	11.25-12.15	12.15-1.00	1.00-1.45	1.45-2.35	2.35-3.25	3.25-4.15
Monday	DSP	SGP	EM-III	EM-III	LUNCH	MPMC	MEA	-----
Tuesday	SGP	EM-III	DSP	MPMC		-----	-----	-----
Wednesday	MPMC	DSP	MEA	SGP		EM LAB-II(A) (INS/BRK) /PE LAB(B) (VVS/CVGK/MDV) /IC LAB(C) (MRR/VRK)		
Thursday	EM-III	SGP	MPMC	DSP		EM LAB-II(B) (INS/NBM) /PE LAB(C) (VVS/CVGK/MDV) /IC LAB(A) (MRR/KNT/VRK)		
Friday	EM LAB-II(C) (INS/NBM) /PE LAB(A) (VVS/CVGK/MDV) /IC LAB(B) (MRR/KNT)			EM-III		MEA	MEA	-----

A,B,C in brackets indicate batches

Legend:

S. No.	Subject Code	Subject		Staff Name
1	EE 351	DSP	Digital Signal Processing	Mr. G. Satyanarayana / Dr. G. Ravindranath
2	EE 352	EM-III	Electrical Machinery-III	Mr. I. Narasimha Swamy
3	EE 353	SGP	Switchgear and Protection	Mr. S. Shyam Mohan
4	EE 354	MPMC	Microprocessors and Microcontrollers	Mr. P.V.V. Raghava Sharma
5	CM 371	MEA	Managerial Economics and Accountancy	Mr. M. Sriranga Raju
6	EE 381	EM LAB – II	Electrical Machines Lab – II	Mr. I. Narasimha Swamy/ Mr. N. Bharat Mohan/ Mr. B. Ramakrishna
7	EE 382	PE LAB	Power Electronics Lab	Mr. C.V.G.K.Rao/ Mr. V.V. Satyanarayana Akula /Ms. M Divya Vani
8	EE 383	IC LAB	Integrated Circuits Lab	Mr. M. Raveendra Reddy/ Ms. K. Navya Tejaswini / Mr. V. Raghukrishna

Timetable coordinator **Chief Timetable Coordinator** **HOD (EEE)** **Principal**

MVSR ENGINEERING COLLEGE – NADERGUL
Department of Electrical & Electronics Engineering
Time Table for IV/IV B.E. II Semester EEE (Sec-A) 2017-2018

Room No: M-102 w.e.f. 08/01/2018

	9.45-10.35	**10.35-11.25**	**11.25-12.15**	**12.15-1.00**	**1.00-1.45**	**1.45-2.35**	**2.35-3.25**	**3.25-4.15**
Monday	PROJECT				LUNCH	PROJECT		
Tuesday	IAFM	UT	DMM	RES		SEMINAR (CVGK/PBGP/DVM)		
Wednesday	UT	UT	DMM	DMM		DSP LAB (A) (GSN/PVVR/DSP)		
Thursday	DSP LAB (B) (GSN/KNT)			UT		RES	IAFM	IAFM
Friday	RES	RES	IAFM	DMM		DSP LAB (C) (GSN/KNT/INS)		

A,B,C in brackets indicate batches

Legend:

S. No.	**Subject Code**	**Subject**		**Staff Name**
1	EE 451	UT	Utilization	Mr. M. Raveendra Reddy
2	CE 452	DMM	Disaster Mitigation and Management	Mr. Ankit Kumar Goyal
3	EE 471	RES	Renewable Energy Sources	Mr. P.B.Guru Prasanna
4	ME 472	IAFM	Industrial Administration and Financial Management	Mr. V. Nikhil Murthy
5	EE 481	DSP LAB	Digital Signal Processing Lab	Mr. G. Satyanarayana/ Ms. K. Navya Tejaswini / Mr. P.V.V.Raghava Sharma / Mrs. D. Sai Prasanna / Mr. I. N Swamy
6	EE 482	PROJECT	PROJECT	Mr. C.V.G.K. Rao /Mr. P.B. Guru Prasanna / Dr. DVM Chary
7	EE 483	SEMINAR	SEMINAR	Mr. C.V.G.K. Rao /Mr. P.B. Guru Prasanna / Dr. DVM Chary

Timetable coordinator **Chief Timetable Coordinator** **HOD (EEE)** **Principal**

MVSR ENGINEERING COLLEGE – NADERGUL
Department of Electrical & Electronics Engineering
Time Table for IV/IV B.E. II Semester EEE (Sec-B) 2017-2018

Room No: M-103 w.e.f. 08/01/2018

	9.45-10.35	**10.35-11.25**	**11.25-12.15**	**12.15-1.00**	**1.00-1.45**	**1.45-2.35**	**2.35-3.25**	**3.25-4.15**
Monday	PROJECT				LUNCH	PROJECT		
Tuesday	RES	IAFM	DMM	UT		DSP LAB (A) (PVVR/GSN/DSP)		
Wednesday	DMM	RES	RES	UT		SEMINAR (DHK/YLN/EVCS)		
Thursday	UT	IAFM	IAFM	RES		DSP LAB (B) (PVVR/GS)		
Friday	DSP LAB (C) (PVVR/DSP)			IAFM		UT	DMM	DMM

A,B,C in brackets indicate batches

Legend:

S. No.	**Subject Code**	**Subject**		**Staff Name**
1	EE 451	UT	Utilization	Mr. M. Raveendra Reddy
2	CE 452	DMM	Disaster Mitigation and Management	Dr. A. Manjunath
3	EE 471	RES	Renewable Energy Sources	Mr. P.B.Guru Prasanna
4	ME 472	IAFM	Industrial Administration and Financial Management	Mr. G. Rajesh Babu
5	EE 481	DSP LAB	Digital Signal Processing Lab	Mr. P.V.V.Raghava Sharma / Mrs. D. Sai Prasanna /Mr. G. Satyanarayana/ Ms. G. Sirisha
6	EE 482	PROJECT	PROJECT	Dr. D. Harikrishna/ Mr. Y.L.N. Rao/ Dr. EVC Sekhara Rao
7	EE 483	SEMINAR	SEMINAR	Dr. D. Harikrishna/ Mr. Y.L.N. Rao/ Dr. EVC Sekhara Rao

Timetable coordinator **Chief Timetable Coordinator** **HOD (EEE)** **Principal**