Code No. 6469 / N

FACULTY OF INFORMATICS

B.E. 4/4 (IT) I-Semester (New) (Main) Examination, November 2013

Subject : VLSI Design

Time : 3 Hours **Max. Marks: 75**

Note: Answer all questions of Part - A and answer any five questions from Part-B.

PART – A (25 Marks)

1. Draw the CMOS logic schematic for f = $\overline{ab+cd}$ and f = $\overline{(a+b)(c+d)}$ (2)
2. Draw the CMOS logic diagram for a non-inverting buffer. (3)
3. What is lithography? (2)
4. List out the advantages of silicon on insulator (SOI) technology over twin tub process. (2)
5. Draw RC switch model equivalent for the CMOS. (3)
6. Write brief note on cell based design with examples. (3)
7. Write the advantages of pseudo NMOS over CMOS. (2)
8. Write the difference between SRAM and DRAM. (3)
9. Explain how to manifest the manufacturing defects in VLSI circuits. (3)
10. Write the salient features of verilog modeling. (2)

PART – B (50 Marks)

11.(a) Explain the electrical characteristics of MOSFET and also derive the relationship between V_{ds} & I_{ds}. (6)
(b) Explain Bubble pushing and pass characteristics of MOSFET. (4)

12.(a) Draw the layouts for series and parallel connected FETs. (6)
(b) Draw the layout of the following basic structures
(i) n well (2)
(ii) Mask for nFET (2)

13. Explain the steps involved in CMOS fabrication process with neat diagrams. (10)

14.(a) Explain the voltage transfer characteristics of CMOS inverter with neat diagrams. (5)
(b) Explain the problems involved in driving large capacitive loads. (5)

15.(a) Explain Domino logic networks and differential cascade voltage switch logic. (5)
(b) Write notes on 1T RAM cell and physical design of DRAM cells. (5)

16.(a) Explain VLSI design flow with neat diagram. (4)
(b) Write notes on floor planning and routing. (6)

17.(a) Write behavioural description of Ripple carry adders. (5)
(b) Draw CMOS schematic and layout diagram for an inverter. (5)

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Code No. 6224 / O

FACULTY OF INFORMATICS

B.E. 4/4 (IT) I-Semester (Old) Examination, November 2013

Subject : VLSI Design

Time : 3 Hours **Max. Marks: 75**

Note: Answer all questions of Part - A and answer any five questions from Part-B.

PART – A (25 Marks)

1. What is Moore's Law? Give n-most transistor current equation. (2)
2. Implement 2 to 1 multiplexer using TG logic? Give its Truth table. (3)
3. What is mean by stick diagram? Draw stick diagram of NOR2 logic. (3)
4. How latch up problem occur in CMOS inverter? Give the latch up prevention technique. (3)
5. What is Yield? Discuss in brief. (2)
6. Define Fan in, Fan out, rise time and fall time. (2)
7. Explain charge sharing mechanism dynamic CMOS logic. (3)
8. Mention differences between SRAM and DRAM. (2)
9. What are blocking and non-blocking assignments? (2)
10. Define sheet resistance. (3)

PART – B (50 Marks)

11.(a) Implement XOR and XNOR logic using TG logic. (5)

(b) Design a CMOS circuit for the OAI expressions $y = \overline{(a+b)(a+c)(b+d)}$ use the smallest number of transistors in your design. (5)

12.(a) An inter connect line runs over an insulating oxide layer that is 20,000 A^{o} thick. The line has width of 0.5 μm and is 40 μm long. The sheet Resistance is 25 Ω.
(i) Find the line Resistance (R line)
(ii) Find the line capacitance Cline. [use εox = 3.45 $3x10^{-13}$ F/cm] (6)

(b) Draw the voltage transfer characteristic of a CMOS inverter and explain. (4)

13.(a) What are λ-based design rules? Explain with an example of a simple inverter. (6)

(b) What are delay minimization techniques in CMOS inverter? (4)

14.(a) Draw a 6T SRAM memory cell. Explain its Write and read operation. (5)

(b) Implement a half adder using CMOS logic. (5)

15.(a) What are high speed adders ? Explain about carry look ahead adder. (5)

(b) What is cross talk? Derive the current equation for three line intern connect model. (5)

16.(a) Derive the n MOS transistor current equation in linear and saturation region. (5)

(b) Design XOR - XNOR logic using differential cascode voltage switch logic. (5)

17. Write short notes on the following:
(a) Floor planning and Rouring (3)
(b) Domino logic (3)
(c) Multipliers (4)

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