Code No. 6421 / N

FACULTY OF ENGINEERING

B.E. 4/4 (ECE) I – Semester (New) (Main) Examination, November 2013

Subject : VLSI Design

Time : 3 hours **Max. Marks : 75**

Note: Answer all questions from Part-A. Answer any FIVE questions from Part-B.

PART – A (25 Marks)

1. What are the advantages of verilog HDL over C-programming language? 2
2. Write a verilog program for three input EXOR logic gate in data flow modeling. 3
3. What are conditional statements in verilog? Give one example. 2
4. Difference between Mealy and Moore model. 2
5. Draw the structure of MOS transistor in enhancement mode for the value of $V_{gs} > V_t$ and $V_{ds} > V_{gs} - V_t$. 2
6. What are the advantages of transmission gate logic over CMOS logic? 2
7. Distinguish between CMOS technology and Bi-CMOS technology. 3
8. What is the effect of threshold voltage on channel length and body effect? 3
9. What is carry skip adder? Give one example. 3
10. Draw IT dynamic RAM read and write operation. 3

PART – B (50 Marks)

11.a) What are data types which used in verilog? Explain. 4
b) Write verilog code for two input OR logic, AND logic and NOT logic using NAND gates. Check the functionality of these gates with a stimulus module. 6

12.a) Describe multiway branching, using case, case x and case z statements. 7
b) Differences between tasks and functions. 3

13.a) How a MOS transistor behaves in enhancement and depletion modes? Explain with help of V-I characteristics (Assume n-channel transistor). 6
b) Implement the function $f(A,B,C,D) = \overline{(AB+C)D}$ using CMOS logic. Explain its operation. 4

14.a) Draw and explain nMOS fabrication process. 6
b) What is the difference between stick diagram and layout diagram. Draw stick diagram of a CMOS inverter. 4

15.a) With help of circuit diagram, explain 4-bit barrel shifter. 5
b) Design D-Flip-Flop using transmission logic gate. 5

16.a) How to estimate the delay of CMOS inverter? Give the procedure to obtain the delay. 6
b) Draw NOR based ROM memory. Explain its operation. 4

17. Write short notes on :
a) Synthesis design flow 4
b) Sequential and parallel blocks 3
c) 6T SRAM cell 3

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