Code No. 6032

FACULTY OF INFORMATICS

B.E. 2/4 (IT) I – Semester (Main) Examination, November 2013

Subject : Digital Electronics and Logic Design

Time : 3 hours **Max. Marks : 75**

Note: Answer all questions from Part-A. Answer any FIVE questions from Part-B.

PART – A (25 Marks)

1. Using algebraic manipulation prove that $(x + y)(x + \bar{y}) = x$. 2
2. What are the universal gates? Why they are called so? 3
3. Neatly draw the 3 input look-up table (LUT) and explain it. 3
4. What is a combinational circuit? Give some examples. 2
5. Write VHDL code for D flip-flop. 3
6. Define flip-flop, register & shift register. 2
7. Differentiate between Moore FSM & Melay FSM. 2
8. Define state diagram, state table & state assignment. 3
9. Write short notes on clock skew. 3
10. Write the steps involved in synthesis process. 2

PART – B (50 Marks)

11.a) Simplify the four variable function using K-map & implement using basic gates.
$f(x_1,x_2,x_3,x_4) = \Sigma m(1,4,5,6,7,10,11,14)$. 6

b) Find the complement of the function 4
$f(x_1,x_2,x_3) = x_1+x_2x_3$ and show that $f + \bar{f} = 1$

12.a) Draw the general structure of FPGA and show how it can be programmed using JTAG cable. 6

b) What is a macro cell? Give the significance of macro cell in CPLD architecture. 4

13.a) Explain the operation positive type master slave edge trigged D flip-flop. 5

b) Design a 3-bit down counter. Draw timing diagram. 5

14. Design a counter circuit using sequential circuit approach. 10

15. Explain the ASM chart and data path circuit for "Divider Control Operation". 10

16.a) Reduce the following function to min-cost SOP and write VHDL code for reduced expression. 7
$f(x_1,x_2,x_3,x_4) = \Sigma m(1,4,7,14,15) + d(0,5,9)$

b) Write short notes on programmable logic devices. 3

17.a) Explain Shannon's expansion theorem. 4
b) Flip-flops Vs Latches 3
c) What are the elements of ASM chart? 3

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