

## FACULTY OF ENGINEERING

B.E. 2/4 (CSE) I-Semester (Main) Examination, November 2013

Subject : Computer Architecture

Time : 3 Hours

Max. Marks: 75

**Note: Answer all questions of Part - A and answer any five questions from Part-B.****PART – A** (25 Marks)

1. Draw a diagram to illustrate the interrupt cycle. (3)
2. The contents of register A is 1101 and that of register 'B' is '0110'. Find the result of the following micro-program sequence (3)
 
$$T_1 : B \leftarrow \bar{B}$$

$$T_2 : EA \leftarrow A + B$$

$$ET_3 : A \leftarrow A + 1$$
3. What are the relative merits of horizontal and vertical micro-instruction format? (2)
4. Express the decimal value  $-0.123$  as a signed – 6 bit number in signed and complement binary formats. What is the maximum error, in using only 5 significant bits after binary point? (3)
5. Draw the space-time diagram of a Instruction pipe line and mention the Hazard possible there in. (3)
6. Compare Isolated and memory mapped I/O. (2)
7. Show the design of a parallel priority with four interrupt devices. (2)
8. Draw the timing diagram for Asynchronous data transfer. (2)
9. A certain memory system has a 128MB main memory and a 2MB. Cache blocks are 32 bytes in size. Show the fields in a memory address if the cache is (i) direct (ii) 8-set associative mapped. (3)
10. Explain the concept of memory hierarchy. (2)

**PART – B** (5x10=50 Marks)

11. Draw the block diagram of a bus system connected to four register with information transferred serially from any register to any other register. Use a decoder and multiplexer to select the source register and a decoder to select destination register.
12. A computer has six timing signals  $t_0$ - $t_5$  (similar to basic computer) and only one flip-flop 'f' for cycle control. When  $f=0$ , control performs the fetch and indirect cycle (if necessary). When  $f=1$ , it executes the instruction. List all control functions and micro operations for the computer when  $F=0$ .
13. A high speed combinational multiplier is to be pipelined in two stages. The first stage is to be bit pair multiplier and multiplication. The second stage is a carry-save adder that produces final product. Taking a case of 32x32 multiplier estimate the propagation delay. Assuming the delay through full adder is 3-gate delays.
14. (a) Explain pipeline for floating point addition and subtraction.  
(b) Draw the circuit of a BCD adder / subtracter and explain its operation.
15. (a) Explain the method of Interrupt driven I/O transfer what are the methods of priority interrupt structures.  
(b) Write about synchronous data communication.
16. (a) A certain 2-way set Associative cache has an access time of 4ns. Compared to a miss time of 60ns. Without the cache, main memory access time was 50 ns. Running a system with and without cache indicate the speed up and hit ratio.  
(b) Explain the concept of Virtual memory.
17. Write short notes on
  - (a) Characteristics of RISC
  - (b) IO processor