



Code No. : 6421/N/S

FACULTY OF ENGINEERING
B.E. 4/4 (ECE) I Semester (New) (Suppl.) Examination, July 2014
VLSI DESIGN

Time : 3 Hours]

[Max. Marks : 75

Note : Answer **all** questions from Part – **A** and **any five** questions from Part – **B**.

PART – A

1. What are compiler directives ? Are they works in similar in C programming language. 2
2. Write a verilog description for 4-bit adder. 3
3. What is the difference between behavioural modeling and structural modeling ? 2
4. What is mean by blocking statements ? Give one example. 2
5. Give the threshold voltage equation of a nMOS transistor. How it is depends on the channel length ? 3
6. Draw a Bi CMOS inverter and give its truth table with reference to the transistors. 3
7. Draw stick diagram and layout diagram of a simple CMOS inverter. 2
8. How to measure the delay in CMOS circuits ? Explain with an example. 2
9. Draw a Manchester carry chain adder cell. 3
10. Difference between SRAM and DRAM. 3

PART – B

(50 Marks)

11. a) Draw and explain typical design flow for VLSI IC circuit. 4
b) Write the verilog description for the full subtractor module. 6
12. a) What is the difference between blocking assignments and non blocking assignments ? Give one example. 4
b) Design a clock with time period 240 and a duty cycle of 25% by using always and initial statements. The value of clock at time = 0 should be initialized to 0. 6
13. a) Explain the electrical properties of MOS transistor. 4
b) An OAI (OR-And-Inverter) function of the form $f = \overline{(a + b)(b + c).d}$ is build using CMOS logic. Design the circuit using CMOS logic. 6



14. a) What are-Lambda-based design rules ? 5
b) How to measure the sheet resistance of a given material ? How the sheet resistance depends on the technology change ? 5
15. a) Design 4×1 multiplexer using transmission gate logic. Explain its operation. 5
b) Explain the 6T SRAM Read and write operation. 5
16. a) Design a NAND based ROM memory cell and explain its operation. 5
b) Write a verilog code for D-flip-flop. Give its simulation results. 5
17. Write a short notes on :
a) Stic diagram of NAND gate. 3
b) Mealy model. 3
c) Body effect 2
d) Gate level Netlist. 2
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