FACULTY OF ENGINEERING
B.E. 3/4 (EE/Inst.) I – Semester (Supplementary) Examination, July 2014

Subject : Digital Electronics and Logic Design

Time : 3 hours   Max. Marks : 75

Note: Answer all questions from Part-A. Answer any FIVE questions from Part-B.
PART – A (25 Marks)

1   Define incompletely specified function.   3
2   Reduce the expression $f = \left(A + \overline{\overline{BC}}\right)\left(A\overline{B} + ABC\right)$.   2
3   What are the applications of multiplexer?   2
4   Define the terms : i) propagation delay   ii) fan-in and   iii) Noise margin   3
5   How does the look ahead carry adder speeds up the addition process?   2
6   Give the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction
      i)   X-Y and   ii) Y-X by using 2's complement method.   3
7   Explain about debouncing switch.   3
8   Define ring counter.   2
9   What is state diagram? Give an example.   3
10 List out the applications of registers.   2

PART – B (50 Marks)

11 Reduce the following function to SOP and POS forms using K-map.   10
    $f(A, B, C, D) = \sum(1, 3, 4, 7, 11) + d(5, 12, 13, 14, 15)$

12 Minimize the following function using the tabular method   10
    $f(A, B, C, D) = \sum(2, 4, 6, 8, 9, 10, 12, 13, 15)$

13 a) Draw the logic diagram and implement the 4-bit magnitude comparator.   6
    b) Realize a full adder using NAND gates.   4

14 a) Explain the operation of positive edge triggered SR flip-flop.   5
    b) Describe about general BCD counter.   5

15 Implement the following function using PLC   10
      $f_1(A, B, C, D) = \sum(0, 1, 2, 3, 6, 9, 11)$
      $f_2(A, B, C, D) = \sum(0, 1, 6, 8, 9)$
      $f_3(A, B, C, D) = \sum(2, 3, 8, 9, 11)$

16 a) Explain about TTL subfamilies.   5
    b) Discuss the steps involved in synthesis procedure using flip-flops.   5

17 a) Expand $A\left(\overline{B} + A\right)$ to maxterms and minterms.   5
    b) Explain about basic latch circuit operation.   5

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