Code No. 6341 / M

FACULTY OF ENGINEERING

B.E. 3/4 (ECE) II – Semester (Main) Examination, June 2014

Subject: Computer Organization and Architecture

Time: 3 Hours **Max.Marks: 75**

Note: Answer all questions from Part A. Answer any five questions from Part B.

PART – A (25 Marks)

1 Define computer organization and computer architecture. (2)
2 Represent the number $(+46.5)_{10}$ as a floating point binary number with normalized faction mantissa 16 bits and exponent 8 bits. (3)
3 Define micro operation and micro instruction. (2)
4 Draw the timing diagram for the following control operation. $C_7T_3 : SC \leftarrow 0$. (3)
5 What are the basic differences between a branch instruction, a call subroutine instruction, and program interrupt. (3)
6 Determine the number of clock cycles to process 200 tasks in a six-segment pipeline. (2)
7 What is the difference between isolated I/0 and memory-mapped I/0. (2)
8 Explain the need for an I/0 interface. (3)
9 What is the advantage of direct mapping over associative mapping in Cache memory organization? (3)
10 Draw the block diagram of a memory table for mapping a virtual address. (2)

PART – B (50 Marks)

11 (a) Draw the flow chart for a sign magnitude addition and subtraction algorithm. (4)
(b) Explain the Booth's multiplication with an example. (6)

12 (a) Explain the all addressing modes of a basic computer. (6)
(b) Explain the operation of a address sequencer in a micro programmed control unit. (4)

13 (a) Explain various phases of an instruction cycle in detail. (6)
(b) A non-pipeline system takes a 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved? (4)

14 (a) Explain the operation of Daisy chaining method of priority interrupt. (6)
(b) Write the sequence of steps to be followed for DMA transfer. (4)

15 (a) Explain the virtual memory concept with block diagram. (6)
(b) Draw the diagram showing the memory connections to CPU. (4)

16 Explain the various elements of Cache design and various mapping techniques used with Cache. (10)

17 Write a brief note about any two of the following: (10)
a) Non-restoring division b) Array processors c) Asynchronous data transfer.

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