Code No. 6032 / S

FACULTY OF INFORMATICS

B.E. 2/4 (IT) I-Semester (Suppl.) Examination, July 2014

Subject : Digital Electronics and Logic Design

Time : 3 Hours **Max. Marks: 75**

Note: Answer all questions of Part - A and answer any five questions from Part-B.

PART – A (25 Marks)

1 State De Morgan's theorems. (2)
2 Implement the function f= $f = \bar{x}_1 + x_1.x_2$ using basic logic gates. (3)
3 Implement XNOR gate using NOR gates only. (2)
4 Compare and contrast between CPLDs and FPGAs. (2)
5 Design a full adder circuit. (2)
6 Give the significance of macro cell. (3)
7 Distinguish between edge triggering and level triggering. (2)
8 Summarize the steps involved in designing a synchronous sequential circuits. (3)
9 List the elements involved in ASM charts. (3)
10 Illustrate static hazard with an example.

PART – B (50 Marks)

11 (a) Realize the switching function after simplification (5)
$f(x_1, x_2, x_3) = \sum m(0, 1, 2, 3)$
(b) Using algebraic manipulations show that for three input variables x_1, x_2 and x_3 (5)
$\pi M(0, 1, 2, 3, 4, 5,6) = x_1x_2x_3$

12 (a) Explain the structure of FPGA. (5)
(b) Find the minimum cost SOP and POS form for the function f
$f(x_1, x_2, x_3) = \sum m(1, 4, 7) + D(2, 5)$

13 (a) Explain the operation of a basic SR latch and write its truth table. (5)
(b) Design 4-bit shift register. (5)

14 Explain state table reduction and state assignment problem with an example. Assume a suitable state table as required. (10)

15 (a) Distinguish between Moore and Mealy model of an FSM. (5)
(b) Draw the circuit of an up counter or down counter and explain. (5)

16 Explain the algorithm for multiplication using ASM chart and data path circuit. (10)

17 Write short notes on the following: (10)
(a) Use of CAD tools in digital design
(b) Different flip-flops, truth table and excitation tables

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