Code No. 6028 / S

# FACULTY OF ENGINEERING

## B.E. 2/4 (CSE) I – Semester (Suppl.) Examination, July 2014

### Subject: Computer Architecture

**Time: 3 Hours** **Max.Marks: 75**

***Note: Answer all questions from Part A. Answer any five questions from Part B.***

**PART – A (25 Marks)**

| | | |
|---|---|---|
| 1 | What is meant by Pipelining? | (2) |
| 2 | Mention different schemes to reduce pipeline branch penalties. | (2) |
| 3 | What is cache miss and cache hit penalty? | (3) |
| 4 | What is meant by basic computer instruction format? | (3) |
| 5 | Define Micro instruction set. | (2) |
| 6 | What is Data Manipulation? | (3) |
| 7 | How super computers differ from Micro computer? | (3) |
| 8 | Define Handshaking? | (2) |
| 9 | Define virtual memory? | (2) |
| 10 | Define page replacement technique and its types. | (3) |

**PART – B (50 Marks)**

11 Explain instruction cycle with the help of flowchart. (10)

12 Explain Booth's Algorithm with an example. (10)

13 How the performance of processor is enhanced with the help of pipelining? Give answer with an example. (10)

14 Explain the following terms with an example
   a) Multiplexer (5)
   b) Full adder (5)

15 Compare the relative merits of the three cache memory organization (10)
   a) Direct mapping cache
   b) Fully associative cache
   c) Set associative cache

16 Explain Hardwired control unit and micro programmed control unit. (10)

17 Explain the concept of FIFO page replacement algorithm. Implement LRU algorithm for the following page trace with the frame size 4.
   0 1 3 6 2 4 5 2 5 0 3 1 2 5 4 1 0 (10)

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